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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/089,904

04/03/2002

Eric Stephen Carlsgaard

RCA 09265

1248

7590

12/28/2005

Joseph S Tripoli
Thomson Multimedia Licensing
P O Box 5312
Princeton, NJ 08540-5312

EXAMINER

KOSTAK, VICTOR R

ART UNIT

PAPER NUMBER

2614

DATE MAILED: 12/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/089,904	CARLSGAARD ET AL.	
	Examiner	Art Unit	
	Victor R. Kostak	2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 17 October 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-12 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,2,5-7,9,11 and 12 is/are rejected.
- 7) ☒ Claim(s) 3, 4, 8 and 10 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

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1. Applicant's arguments with respect to the rejection based on Nakano (and secondary references), in light of the amendment, have been considered but are moot in view of the new ground(s) of rejection. Applicant's arguments are addressed in the context of the rejection.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 2 and 5 are again rejected under 35 U.S.C. 102(b) as being anticipated by Nakano.

Reviewing the system of Nakano (noting particularly Fig. 6), it includes a signal input for receiving an analog signal having a synchronizing characteristic (RF signal sent to elements 5-7; col. 4 lines 6-14 describing sync data of the input signal); a first reference clock generator arrangement (22, 23) that is based on the disk medium and independent of the input signal; a second reference clock generator arrangement (24, 25) coupled to and a function of the first clock generator arrangement; signal processing section (5, 6, 9) including plural A/D convertors 5 and 6 that are coupled and responsive to the second clock generator arrangement (in which the second clock is independent of the input signal, as noted previously), for sampling and processing the input analog signal in accordance with a sampling rate and an appropriate signal standard (an inappropriate standard would not provide adequate system operation); wherein the sampling frequency of the A/D convertors assume that of the second clock generator arrangement, as shown.

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Applicant basically argues that since clock signals G and I (initially described in reference to the arrangement shown in Fig. 1) are generated by clock pit extraction component 22 (in the embodiment shown in Fig. 6), then they are fundamentally derived from the original input signal stored on the disk, which therefore indicates that the pair of clock signals cannot be considered being independent of a synchronization characteristic of the input analog signal.

The examiner counters by pointing out that the arrangement shown in Fig. 6 in fact has separate signals at separate respective inputs. A first input signal is applied to stage 22 and a second input signal (corresponding to applicant's claimed "*signal input ...synchronizing characteristic*") is applied to parallel stages 5-7. A reasonable interpretation of applicant's claim 1 and a reasonable application of Nakano's Fig. 6 embodiment allows one of ordinary skill in the art to consider the clock signals as being derived from the first signal applied to input stage 22. The terminal that splits into stages 6-7 can be considered as corresponding to applicant's claimed analog signal input, which is a different input signal from that applied to stage 22. Reference clock signals G and I derived from stage 22 are independent from the other input signal (and accompanying synchronization data) that are separately applied to stages 5-7.

As for the now considered limitation regarding the A/D convertors being clocked by respective plural clock signals, that is met by stages 5 and 6, which operate at frequencies corresponding to their sampling rates (col. 5 lines 8-10). As explained above, their clock signals are independent from the analog input having a synchronization characteristic because they have been derived from a separate and different input signal. Nakano also applied optimal sampling to minimize negative effects on the analog due to digitization (e.g. col. 2 lines 52-56).

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As for claim 2, the processing section (which includes separate parallel channels having separate respective A/D convertors) receives separate analog signals, the analog signals having sync characteristics (noted above), and the reference clock signal (of both the first and second clock arrangements) is independent of the sync characteristics.

As for claim 5, the signal processing section (5,6, 9) extends to a decoding processing stage (not shown), and the processing section processes a digital signal (after the conversion) having a sync characteristic (the digital signal derived from the input analog signal having the sync characteristic), and the reference clock is independent from that sync characteristic since it is derived from the disk medium, explained previously.

3. Applicant argues along the same line regarding the rejection based on obviousness applied to claims 6, 7, 9, 11 and 12. The examiner accordingly counters using the same reason given in the rejection above.

The following rejection is repeated from the last Office action thereby consolidating all issues.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 6, 7, 9, 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of Hedlund et al. (both of record).

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As for claims 6 and 9, since Nakano does not specify the signal type he processes in disk storage system, he thereby gives an implicit suggestion that any well known information signal would have been obvious to store on and reproduce from his disk (his system is designed for real-world signals in practical applications). It would therefore have been obvious to process audio, video and other data types in such a disk recording system, as is taught by Hedlund, who points out that any of various signal types can be recorded and reproduced from disk, and using any suitable manner (col. 2 lines 17-31).

As for claims 7 and 11, the processing section (which includes separate parallel channels having separate respective A/D convertors) receives separate analog signals, the analog signals having sync characteristics (noted above), and the reference clock signal (of both the first and second clock arrangements) is independent of the sync characteristics, as discussed above.

The initially received analog signal can be a television signal, as taught by Hedlund discussed above, thereby meeting claim 12.

1. Claims 3, 4, 8 and 10 remain allowable over the prior art.
2. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period

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will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor R. Kostak whose telephone number is (571) 272-7348. The examiner can normally be reached on Monday - Friday from 6:30am-3:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller can be reached on (571) 272-7353. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this final action should be mailed to:

Box AF
Commissioner of Patents and Trademarks
P.O. Box 1450
Alexandria, Virginia 22313-1450

Or faxed to:

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(571) 273-8300

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Customer Service Office whose telephone number is (703) 308-HELP.

Victor R. Kostak
Primary Examiner
Art Unit 2614

VRK

